IN THE SPECIFICATION

Please amend the paragraph beginning on page 1 at line 10, as follows:

This application is related to U.S. Patent Application No. 10/643,744, entitled "Multistreamed Processor Vector Packing Method and Apparatus", filed on even date herewith; to U.S. Patent Application No. 10/643,577, entitled "System and Method for Processing Memory Instructions", filed on even date herewith; to U.S. Patent Application No. 10/643,742, entitled "Decoupled Store Address and Data in a Multiprocessor System", filed on even date herewith; to U.S. Patent Application No. 10/643,586, entitled "Decoupled Scalar/Vector Computer Architecture System and Method ~~(as amended)~~", filed on even date herewith; to U.S. Patent Application No. 10/643,585, entitled "Latency Tolerant Distributed Shared Memory Multiprocessor Computer", filed on even date herewith; to U.S. Patent Application No. ~~110/643,754~~ 10/643,754, entitled "Relaxed Memory Consistency Model", filed on even date herewith; to U.S. Patent Application No. 10/643,758, entitled "Remote Translation Mechanism for a Multinode System", filed on even date herewith; and to U.S. Patent Application No.10/643,741, entitled "Multistream Processing Memory-And Barrier-Synchronization Method and Apparatus", filed on even date herewith, each of which is incorporated herein by reference.